MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2017/2018

ENT4066 – NANOELECTRONICS MATERIALS AND DEVICES
(NE)

16 OCTOBER 2017
9.00 a.m. – 11.00 a.m.
(2 Hours)

INSTRUCTION TO STUDENTS

1. This examination paper consists of 5 pages with 4 questions only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in the Answer Booklet provided.

QUESTION 1

(a) (i) Define the following terms as in **Table Q1(a)** below:

Table Q1(a)

Term	Definition
Nanocrystal	
Nanocomposite	
Colloid	

[3 marks]

(ii) What are the two different properties of Nano Materials that very much different from the properties of bulk material at a larger scale.

[2 marks]

(iii) Nano particles have a much greater surface area per given volume compared with larger particles. Explain the above statement by assuming a sphere having variable radius "*r*".

[4 marks]

(iv) Name THREE (3) colour generation mechanisms from nanoparticle or nanostructure.

[3 marks]

(b) (i) Briefly explain "Artificial Atoms".

[2 marks]

(ii) Nanostructured materials could have different degrees of freedom. With the aid of relevant diagram briefly explain the density of state (DOS) for nanostructured materials in different degrees of freedom.

[6 marks]

(c) What happens for device sizes comparable to the mean free path, or other length scale, e.g. deBroglie or Fermi wave length?

[3 marks]

(d) What are the key consideration involved in nano particle synthesis.

[2 marks]

Continued.....

QUESTION 2

(a) (i) Briefly Explain what is "Gibbs Free Energy"

[2 marks]

(ii) With the aid of relevant diagram schematically illustrate the process of nucleation and subsequent growth of nanoparticle in liquid phase.

[4 marks]

(b) Briefly explain the distinct steps involved in the sol-gel synthesis process.

[4 marks]

(c) (i) What is the Chiral vector for carbon nanotube (CNT)? [2 marks]

(ii)Write an expression which describes whether a CNT is metallic or semiconducting.

[1 mark]

(iii) The chiral angle (θ) and diameter (d) of a carbon nanotube (CNT) is given by:

$$\theta = tan^{-1}\left[\frac{\sqrt{3}\,m}{m+2n}\right]$$

$$d = \frac{\sqrt{3}\,a_{cc}\sqrt{(m^2+n^2+mn)}}{\pi}$$

respectively, where m and n are integers governing the chiral vector C, and a_{cc} = 0.142 nm is the carbon bond length. A two-dimensional graphene sheet is rolled-up to form 10-μm, (n=6, m=1) single-wall carbon nanotube (SWCNT). Calculate the chiral angle and diameter of the SWCNT.

[4 marks]

(d) Illustrate the E-K and E-DOS diagram of metallic and semiconducting CNT.

[4 marks]

(e) Bandgap energy of CNT varied with the diameter/radius of CNT and energy bandgap of CNT is inversely proportional to the tube diameter. Briefly explain the above statements using Kataura-plot.

[4 marks]

Continued.....

QUESTION 3

(a) For dimensional (1D) materials, explain "Van Hove singularities" with relevant illustration.

[4 marks]

(b) (i) Explain TWO (2) unique properties of Graphene that are not applicable for the standard theory of semiconductors.

[4 marks]

(ii) Large scale manufacturing foundry could utilize Chemical Vapor Deposition (CVD) process to fabricate Graphene. Briefly explain the process steps involved in the fabrication process of Graphene using CVD method.

[6 marks]

(c) Briefly explain Moore's Law. How device scaling is related with Moore's law.

[2 marks]

(d) Assume **Figure Q3(c)** is a scaled device with scaling factor α applied to the device scaling. Draw the original device without applying the scaling factor and explain the relation between the electric field configuration of the original and scaled devices provided in **Figure Q3(c)**.

[3+2 marks]

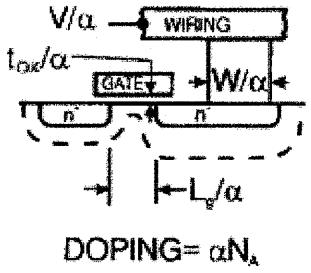

Figure Q3(c): Scaled Device

(e) Explain why any FOUR (4) from the following parameters that do not scale well, which has caused specific problems associated with Small Dimensional Transistors.

(i) Scaling of Subthreshold Current
(ii) Hot Electrons
(iii) Short-Channel Effects and Drain-induced Barrier Lowering
(iv) Narrow-Width Effects
(v) Velocity Saturation
(vi) Source-Drain Resistance

[4 x 1 marks]

Continued.....

QUESTION 4

(a) (i) For an interconnect conducting layer if RC stands for resistance and capacitance respectively, then what is RC delay.

[2 marks]

(ii) Briefly explain why Low-k dielectric materials is used to surrounded the conductor.

[2 marks]

(iii) There are five general requirements for a low-k material to be successfully integrated into the device structures, briefly explain any FOUR (4) of them.

[4 marks]

(b) Quantum effect devices, such as Resonant tunnelling diodes (RTDs) with negative differential resistance (NDR) characteristics, have the potential to improve the circuit performance by combining conventional devices. Briefly Explain how RTDs can be used to improve circuit performance.

[2 marks]

(c) In a single-electron transistor (SET) circuit what is "Coulomb Blockade". For a tiny circuit of SET, why electron must pass one by one.

[4 marks]

(d) Briefly Explain THREE (3) main components used in Organic Field Effect Transistor (OFET) and illustrate THREE (3) popular organic-transistor geometries.

[6 marks]

(e) (i) By mean of simple diagrams, compare the current-voltage characteristic of a normal capacitor and a quantum-dot capacitor.

[2 marks]

(ii) Consider a single-electron transistor (SET) consists of a nanosized capacitance having $C=2\pi\varepsilon\varepsilon_o d$, where d (12 nm) is the diameter of island, $\varepsilon=4$ and $\varepsilon_o = 8.89\text{x}10^{-12}$Fm. Calculate the temperature limit for SET effect. Given that Boltzmann's constant is $1.38066\text{x}10^{-23}$ J/K.

[3 marks]

End of Paper